REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on November 12, 2002.

Pat Slaback
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Signature

VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

41. (Amended) The [method] programmable logic device of Claim 40, further comprising means for converting the PMA reference clock signal to a lower voltage signal for use in a physical coding sublayer of the multi-gigabit transceiver.

42. (New) A system, comprising:

a programmable logic device including:

programmable input/output circuitry,

programmable core logic coupled to the programmable input/output circuitry,

a multi-gigabit transceiver coupled to the programmable core logic,

a first pair of clock pads, and

a dedicated routing structure directly connecting the first pair of clock pads and the multi-gigabit transceiver; and

a clock generation circuit coupled to the first pair of clock pads.

43. (New) The system of Claim 42, wherein the dedicated routing structure comprises:

a differential buffer coupled to the first pair of clock pads; and

a first clock trace providing a direct connection between the differential buffer and the multi-gigabit transceiver.

44. (New) The system of Claim 42, wherein the programmable logic device further comprises:

a second pair of clock pads; and

a second dedicated routing structure directly connecting the second pair of clock pads and the multi-gigabit transceiver.

45. (New) The system of Claim 44, wherein the second dedicated routing structure comprises:

a second differential buffer coupled to the second pair of clock pads; and

a second clock trace providing a direct connection between the second differential buffer and the multi-gigabit transceiver.

46. (New) The system of Claim 45, wherein the programmable logic device further comprises a first multiplexer coupled to the first and second clock traces, the first multiplexer being configured to selectively route a clock signal on either the first or second clock trace in response to a select signal.

47. (New) The system of Claim 46, wherein the programmable logic device further comprises a programmable connection between the programmable core logic and the first multiplexer, wherein the programmable core logic provides the select signal to the first multiplexer.

48. (New) The system of Claim 46, wherein the first multiplexer comprises:

a first transmission gate configured to be enabled in response to the select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to receive a clock signal on the second clock trace and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

49. (New) The system of Claim 46, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the first multiplexer.

50. (New) The system of Claim 49, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the first multiplexer.

51. (New) The system of Claim 42, wherein the programmable logic device further comprises:

a first general-purpose clock pad;

a first down-level shifter coupled to the first general-purpose clock pad; and

a general-purpose clock routing path coupling the down-level shifter to the multi-gigabit transceiver.

52. (New) The system of Claim 51, wherein the programmable logic device further comprises a multiplexer coupled to the dedicated routing structure and the general-purpose clock routing path, the multiplexer being configured to selectively route a clock signal on either the dedicated routing structure or the general-purpose clock routing path in response to a select signal.

53. (New) The system of Claim 52, wherein the programmable logic device further comprises a first configuration memory cell that is programmable to store and provide the select signal.

54. (New) The system of Claim 52, wherein the multiplexer comprises:

a first transmission gate configured to be enabled in response to the select signal;

a second transmission gate configured to be enabled in response to the inverse of the select signal;

a first logic gate having input terminals coupled to receive a clock signal on the dedicated routing structure and the select signal, and an output terminal coupled to the first transmission gate; and

a second logic gate having input terminals coupled to receive a clock signal on the general-purpose clock routing path and the inverse of the select signal, and an output terminal coupled to the second transmission gate.

55. (New) The system of Claim 52, wherein the multi-gigabit transceiver comprises a phase locked loop configured to receive the clock signal selected by the multiplexer.

56. (New) The system of Claim 55, wherein the multi-gigabit transceiver further comprises a serializer configured to operate in response to a serializing clock signal generated by the phase locked loop in response to the clock signal selected by the multiplexer.

57. (New) The system of Claim 42, wherein the multi-gigabit transceiver comprises a physical media access (PMA) sublayer and a physical coding sublayer (PCS).

58. (New) The system of Claim 57, wherein the programmable logic device further comprises means for routing a clock signal on the dedicated routing structure to a phase locked loop in the PMA as a PMA reference clock signal.

59. (New) The system of Claim 58, wherein the programmable logic device further comprises a down-level shifter configured to receive the PMA reference clock signal, and in response, provide a PCS reference clock signal to the PCS.

60. (New) The system of Claim 42, wherein the first pair of clock pads is located near the center of an edge of the programmable logic device.